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DigiPEG v1.6

Connectors and pin description

Rev G, January, 31 2006

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Revision history:

Rev A, January, 14 2003, abesani@tecnoroll.it

First release

Rev B, May, 8 2003, abesani@tecnoroll.it

Added DigiPEG block diagram

Rev C, July, 25 2003, abesani@tecnoroll.it

Added pin definition for service channel serial port

Rev D, February, 8 2004, abesani@tecnoroll.it

Cleaned up definition for service channel serial port

Rev E, July, 27 2004, abesani@tecnoroll.it

Fixed an incorrect label on CN6 description

Added a note on digital audio connections

Added power characteristics for MB86391 boards

Rev F, December, 23 2004, abesani@tecnoroll.it

Added documentation for PCB revision 1.4

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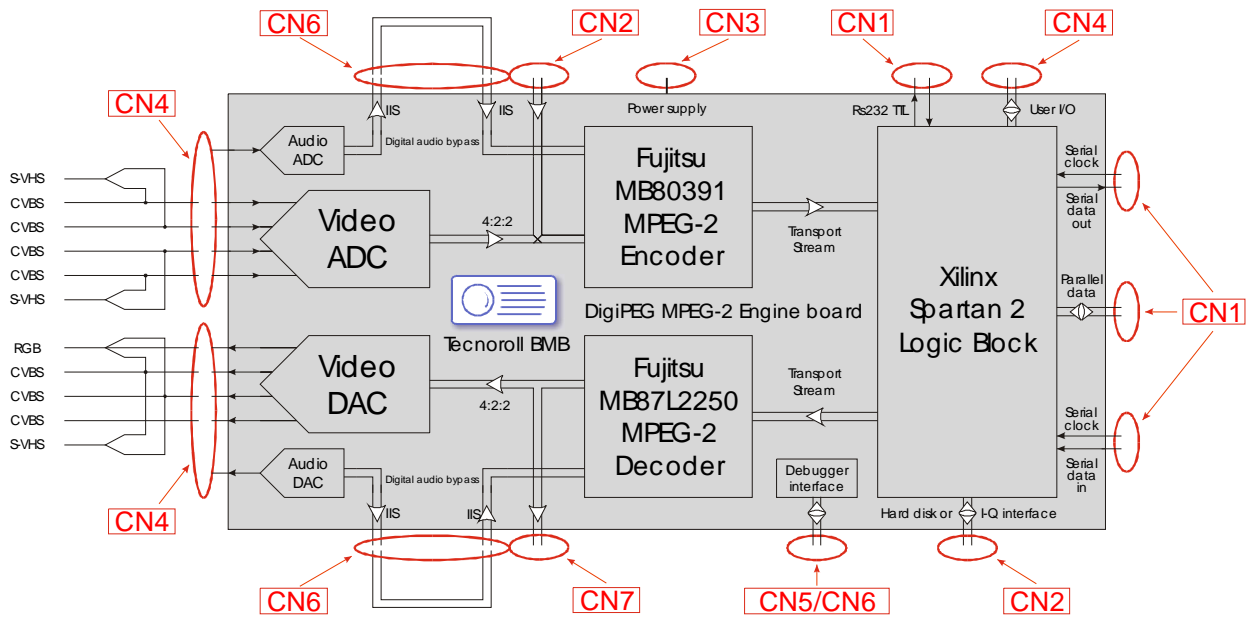
Added documentation for PCB revision 1.6

Added DigiPEG board layouts

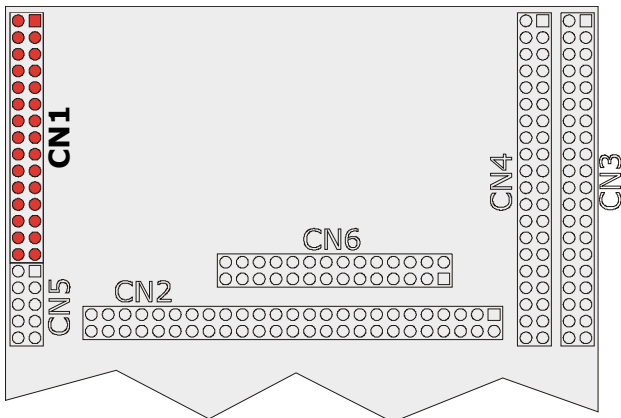
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1. DigiPEG block connection diagram



2. CN1 (Transport Stream I/O, control I/O)

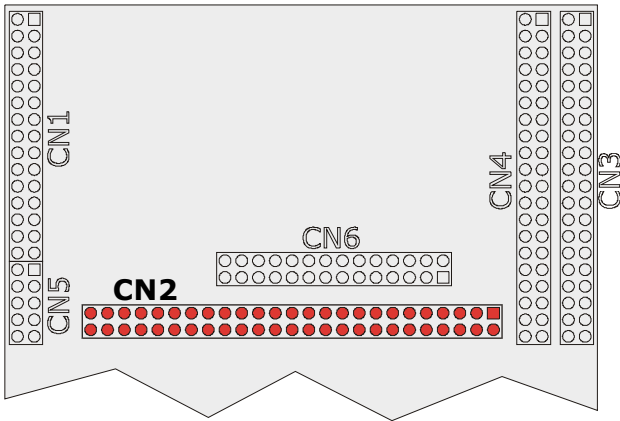


CN1 position, viewed from connector solder side.

CN1 (TS I/O, ASI out, I/O)			
Pin	Symbol	I/O/P	Description
1	GNDD	P	Digital ground
2	GNDD	P	Digital ground
3	SER_TX_CLK	I	Serial Transport Stream TX clock input
4	SER_RX_CLK	I	Serial Transport Stream RX clock input

CN1 (TS I/O, ASI out, I/O)			
Pin	Symbol	I/O/P	Description
5	SER_TX_DATA	O	Serial Transport Stream TX data output
6	SER_RX_DATA	I	Serial Transport Stream RX data input
7	SERV_CLK	I/O	DevBoard XBus clock line
8	SERV_CS	I/O	DevBoard XBus CS line
9	SERV_DATA	I/O	DevBoard XBus Data line
10	TS_VALID	I/O	Parallel Transport Stream VALID signal
	ASI_ENA	O	ASI Write ENable output
11	TS_CLK	I/O	Parallel Transport Stream CLOCK signal
12	TS_PSTART	I/O	Parallel Transport Stream PSTART (or PSYNC) signal
	ASI_CLK_OUT	O	ASI write clock output
13	5V0	P	+5.0V Power supply
14	5V0	P	+5.0V Power supply
15	USER_TX	O	User RS232 TX line
16	USER_RX	I	User RS232 RX line
17	TS_D0	I/O	Parallel Transport Stream Data line, bit 0
	ASI_OUT_D0	O	Deserialized ASI output bit 0
18	TS_D1	I/O	Parallel Transport Stream Data line, bit 1
	ASI_OUT_D1	O	Deserialized ASI output bit 1
19	TS_D2	I/O	Parallel Transport Stream Data line, bit 2
	ASI_OUT_D2	O	Deserialized ASI output bit 2
20	TS_D3	I/O	Parallel Transport Stream Data line, bit 3
	ASI_OUT_D3	O	Deserialized ASI output bit 3
21	TS_D4	I/O	Parallel Transport Stream Data line, bit 4
	ASI_OUT_D4	O	Deserialized ASI output bit 4
22	TS_D5	I/O	Parallel Transport Stream Data line, bit 5
	ASI_OUT_D5	O	Deserialized ASI output bit 5
23	TS_D6	I/O	Parallel Transport Stream Data line, bit 6
	ASI_OUT_D6	O	Deserialized ASI output bit 6
24	TS_D7	I/O	Parallel Transport Stream Data line, bit 7
	ASI_OUT_D7	O	Deserialized ASI output bit 7
25	3V3	P	+3.3V Power supply
26	3V3	P	+3.3V Power supply
27	2V5	P	+2.5V Power supply
28	2V5	P	+2.5V Power supply
29	GNDD	P	Digital ground
30	GNDD	P	Digital ground

3. CN2 (Hard Disk)



CN2 connector, viewed from connector solder side.

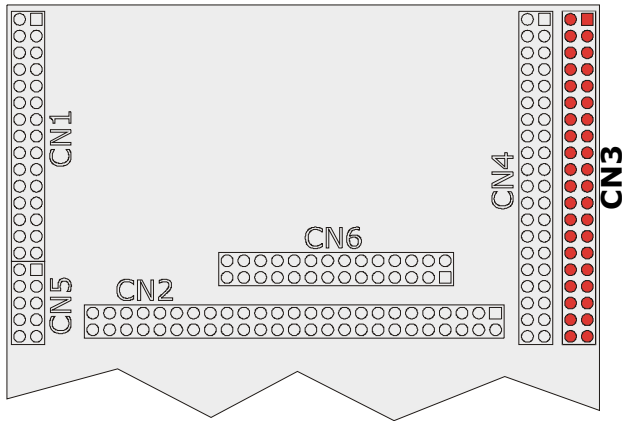
Note that this connector is reversed.

CN2 (Hard disk/ITU656 in/ASI in)			
Pin	Symbol	I/O/P	Description
A	EXT_27MHz_IN	I	External 27Mhz input for the MPEG encoder. Note: to use this 27MHz input, resistor R88 (see <i>DigiPEG board TOP layout</i> on page 16) should be removed, in order to disconnect the internal 27Mhz oscillator.
B	-	-	Not connected
C	-	-	Not connected
D	-	-	Not connected
E	EXT_INT_1	I	DigiPEG external interrupt 1. Active LOW.
F	EXT_INT_0	I	DigiPEG external interrupt 0. Active LOW.
1	HD_RESET	O	Hard disk reset signal. Used for both IDE channels. (RESET-). Active LOW
2	GNDD	P	Digital ground
3	HD_D7	I/O	Hard disk data bus bit 7. Used for both IDE channels. (DD7)
	ASI_IN_D7	I	Deserialized ASI input bit 7
4	HD_D8	I/O	Hard disk data bus bit 8. Used for both IDE channels. (DD8)
5	HD_D6	I/O	Hard disk data bus bit 6. Used for both IDE channels. (DD6)
	ASI_IN_D6	I	Deserialized ASI input bit 6
6	HD_D9	I/O	Hard disk data bus bit 9. Used for both IDE channels. (DD9)
	ASI_IN_CKR	I	ASI recovered clock input
7	HD_D5	I/O	Hard disk data bus bit 5. Used for both IDE channels. (DD5)
	ASI_IN_D5	I	Deserialized ASI input bit 5
8	HD_D10	I/O	Hard disk data bus bit 10. Used for both IDE channels. (DD10)
	ASI_SC/D	I	ASI SpecialCharacter/Data input
9	HD_D4	I/O	Hard disk data bus bit 4. Used for both IDE channels. (DD4)
	ASI_IN_D4	I	Deserialized ASI input bit 4

CN2 (Hard disk/ITU656 in/ASI in)			
Pin	Symbol	I/O/P	Description
10	HD_D11	I/O	Hard disk data bus bit 11. Used for both IDE channels. (DD11)
	ASI_27Mhz	O	Optional ASI 27Mhz reference output
11	HD_D3	I/O	Hard disk data bus bit 3. Used for both IDE channels. (DD3)
	ASI_IN_D3	I	Deserialized ASI input bit 3
12	HD_D12	I/O	Hard disk data bus bit 12. Used for both IDE channels. (DD12)
13	HD_D2	I/O	Hard disk data bus bit 2. Used for both IDE channels. (DD2)
	ASI_IN_D2	I	Deserialized ASI input bit 2
14	HD_D13	I/O	Hard disk data bus bit 13. Used for both IDE channels. (DD13)
15	HD_D1	I/O	Hard disk data bus bit 1. Used for both IDE channels. (DD1)
	ASI_IN_D1	I	Deserialized ASI input bit 1
16	HD_D14	I/O	Hard disk data bus bit 14. Used for both IDE channels. (DD14)
17	HD_D0	I/O	Hard disk data bus bit 0. Used for both IDE channels. (DD0)
	ASI_IN_D0	I	Deserialized ASI input bit 0
18	HD_D15	I/O	Hard disk data bus bit 15. Used for both IDE channels. (DD15)
19	GNDD	P	Digital ground
20	HD_KEY	-	Do not connect
	ITU656_CLK	I	ITU656 Clock input. Note: to use this clock input, resistor R80 (see <i>DigiPEG board BOTTOM layout</i> on page 17) should be removed in order to disconnect the internal IAD_CLK_OUT from ITU656_CLK input.
21	HD_DMARQ	I	Not used, since only PIO modes are used by DigiPEG.
	SCL2	I/O	Secondary I ² C bus clock line.
22	GNDD	P	Digital ground
23	HD_IOWR	O	Hard disk I/O write signal. Used for both IDE channels (DIOW-). Active LOW.
	SDA2	I/O	Secondary I ² C bus data line.
24	GNDD	P	Digital ground
25	HD_IORD	O	Hard disk I/O read signal. Used for both IDE channels (DIOR-). Active LOW.
	ITU656_D7	I	ITU656 input bit 7
26	GNDD	P	Digital ground
27	HD_IORDY	I	Hard disk I/O ready signal. Used for both IDE channels (IORDY).
	ITU656_D6	I	ITU656 input bit 6
28	HD2_CS1	O	Hard disk Chip Select 1 for IDE channel 2 (CS1-). Active LOW.
	AD_RESET	O	External ADC reset line
29	HD_DMACK	O	Not used, since only PIO modes are used by DigiPEG.
	ITU656_D5	I	ITU656 input bit 5
30	GNDD	P	Digital ground
31	HD_INTRQ	I	Hard disk interrupt request for IDE channel 1 (INTRQ). Active LOW.
	ITU656_D4	I	ITU656 input bit 4

CN2 (Hard disk/ITU656 in/ASI in)			
Pin	Symbol	I/O/P	Description
32	IAD_CLK_OUT	O	Internal ADC (SAA7113) Clock output
33	HD_A1	O	Hard disk Device address bit 1. Used for both IDE channels (DA1).
	ITU656_D3	I	ITU656 input bit 3
34	HD_PDIAG	I	Not used.
	DVI_SEL0	O	DigitalVideoIn selection bit 0
35	HD_A0	O	Hard disk Device address bit 0. Used for both IDE channels (DA0).
	ITU656_D2	I	ITU656 input bit 2
36	HD_A2	O	Hard disk Device address bit 2. Used for both IDE channels (DA2).
	DVI_SEL1	O	DigitalVideoIn selection bit 1
37	HD_CS0	O	Hard disk Chip Select 0 for IDE channel 1 (CS0-). Active LOW.
	ITU656_D1	I	ITU656 input bit 1
38	HD_CS1	O	Hard disk Chip Select 1 for IDE channel 1 (CS1-). Active LOW.
	Q5	I/O	Not used
39	HD2_INTRQ	I	Hard disk interrupt request for IDE channel 2 (INTRQ). Active LOW.
	ITU656_D0	I	ITU656 input bit 0
40	GNDD	P	Digital ground
41	5V0	P	+5.0V Power supply
42	5V0	P	+5.0V Power supply
43	GNDD	P	Digital ground
44	HD2_CS0	O	Hard disk Chip Select 0 for IDE channel 2 (CS0-). Active LOW.
	Q6	I/O	Not used
S1	-	-	Not connected
S2	-	-	Not connected
S3	-	-	Not connected
S4	-	-	Not connected

4. CN3 (Power supply)



CN3 connector, viewed from connector solder side.

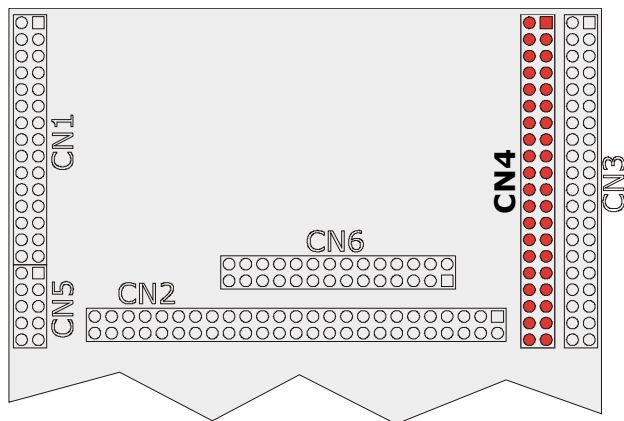
CN3 (Power supply)			
Pin	Symbol	I/O/P	Description
1	GNDA	P	Analog ground
2	1V8	P	+2.5V Power supply / +1.8V Power supply ⁽¹⁾
3	GNDA	P	Analog ground
4	1V8	P	+2.5V Power supply / +1.8V Power supply ⁽¹⁾
5	GNDA	P	Analog ground
6	1V8	P	+2.5V Power supply / +1.8V Power supply ⁽¹⁾
7	GNDA	P	Analog ground
8	2V5	P	+2.5V Power supply
9	GNDA	P	Analog ground
10	2V5	P	+2.5V Power supply
11	GNDA	P	Analog ground
12	2V5	P	+2.5V Power supply
13	GNDD	P	Digital ground
14	VBATT	P	+3.0V for DigiPEG clock/calendar
15	GNDD	P	Digital ground
16	5V0	P	+5.0V Power supply
17	GNDD	P	Digital ground
18	5V0	P	+5.0V Power supply
19	GNDD	P	Digital ground
20	5V0	P	+5.0V Power supply
21	GNDD	P	Digital ground
22	5V0	P	+5.0V Power supply
23	GNDD	P	Digital ground
24	5V0	P	+5.0V Power supply
25	GNDD	P	Digital ground

CN3 (Power supply)			
Pin	Symbol	I/O/P	Description
26	5V0	P	+5.0V Power supply
27	GNDD	P	Digital ground
28	3V3	P	+3.3V Power supply
29	GNDD	P	Digital ground
30	3V3	P	+3.3V Power supply
31	GNDD	P	Digital ground
32	3V3	P	+3.3V Power supply
33	GNDD	P	Digital ground
34	3V3	P	+3.3V Power supply
35	GNDD	P	Digital ground
36	3V3	P	+3.3V Power supply
37	GNDD	P	Digital ground
38	3V3	P	+3.3V Power supply
39	GNDD	P	Digital ground
40	3V3	P	+3.3V Power supply

Notes:

1. 2.5 Volt for boards with the MB86390A encoder, 1.8 Volt for boards with the MB86391 encoder.

5. CN4 (User I/O)



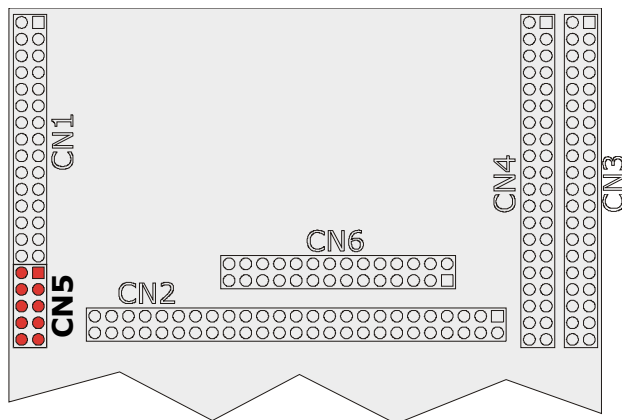
CN4 connector, viewed from connector solder side.

CN4 (User I/O)			
Pin	Symbol	I/O/P	Description
1	GNDA	P	Analog ground

CN4 (User I/O)			
Pin	Symbol	I/O/P	Description
2	AUDIO_OUT_L	O	Analog left channel audio line output
3	GNDA	P	Analog ground
4	AUDIO_OUT_R	O	Analog right channel audio line output
5	GNDA	P	Analog ground
6	CVBS_OUT	O	Analog composite video (CVBS) output. 1Vpp on 75Ω. Used for sync output when RGB output is selected.
7	GNDA	P	Analog ground
8	RED_OUT	O	Analog RED (RGB), Chroma (C, S-VHS) or CVBS video output.
9	GNDA	P	Analog ground
10	GREEN_OUT	O	Analog GREEN (RGB), Luma (Y, S-VHS) or CVBS video output.
11	GNDA	P	Analog ground
12	BLU_OUT	O	Analog BLUE (RGB) output. Not used for S-VHS or CVBS output.
13	GNDA	P	Analog ground
14	AV_IN_0	I	Analog composite video input (CVBS0) or analog Y (luma) input (S-VHS2)
15	GNDA	P	Analog ground
16	AV_IN_1	I	Analog composite video input (CVBS1) or analog Y (luma) input (S-VHS1)
17	GNDA	P	Analog ground
18	AV_IN_2	I	Analog composite video input (CVBS2) or analog C (Chroma) input (S-VHS2)
19	GNDA	P	Analog ground
20	AV_IN_3	I	Analog composite video input (CVBS3) or analog C (Chroma) input (S-VHS1)
21	GNDA	P	Analog ground
22	AUDIO_IN_R	I	Analog right channel audio line input
23	GNDD	P	Digital ground
23	AUDIO_IN_L	I	Analog left channel audio line input
25	GNDD	P	Digital ground
26	EX_CTRL7	I/O	User GPIO pin, bit 7
27	GNDD	P	Digital ground
28	EX_CTRL6	I/O	User GPIO pin, bit 6
29	GNDD	P	Digital ground
30	EX_CTRL5	I/O	User GPIO pin, bit 5. Input for Tx service channel serial port.
31	GNDD	P	Digital ground
32	EX_CTRL4	I/O	User GPIO pin, bit 4. Output for Rx service channel serial port.
33	GNDD	P	Digital ground
34	EX_CTRL3	I/O	User GPIO pin, bit 3. Menu button on DigiPEG DevBoard.
35	GNDD	P	Digital ground

CN4 (User I/O)			
Pin	Symbol	I/O/P	Description
36	EX_CTRL2	I/O	User GPIO pin, bit 2. ESC button on DigiPEG DevBoard.
37	GNDD	P	Digital ground
38	EX_CTRL1	I/O	User GPIO pin, bit 1. Down button on DigiPEG DevBoard.
39	GNDD	P	Digital ground
40	EX_CTRL0	I/O	User GPIO pin, bit 0. Up button on DigiPEG DevBoard.

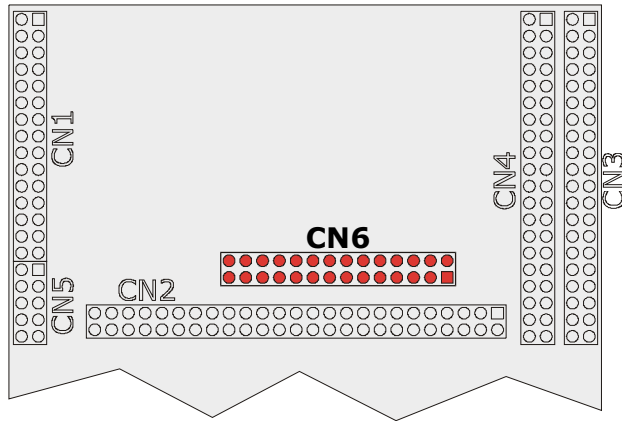
6. CN5 (ARC Debugger interface)



CN5 connector, viewed from connector solder side.

CN5 (ARC debugger interface)			
Pin	Symbol	I/O/P	Description
1	5V0	P	+5.0V Power supply for ARC debugger interface
2	3V3	P	+3.3V Power supply for ARC debugger interface
3	DBG0	I/O	ARC debugger interface I/O line
4	DBG1	I/O	ARC debugger interface I/O line
5	DBG2	I/O	ARC debugger interface I/O line
6	DBG3	I/O	ARC debugger interface I/O line
7	DBG4	I/O	ARC debugger interface I/O line
8	RESET	I/OC	DigiPEG master RESET signal. Active LOW
9	DBG5	I/O	ARC debugger interface I/O line
10	GNDD	P	Digital ground

7. CN6 (Digital Audio, FPGA programming, I/O)



CN6 connector, viewed from connector solder side.

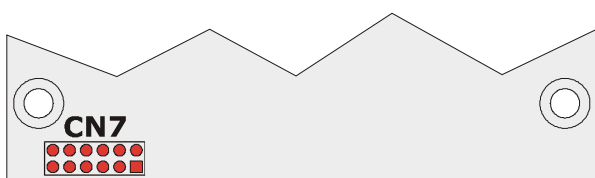
CN6 (Digital Audio, FPGA, I/O)			
Pin	Symbol	I/O/P	Description
1	RU_RXD	I	RS232 Debug Port RX Data line
2	RU_TXD	O	RS232 Debug Port TX Data line
3	RU_AOLRCLK	O	I ² S LRCLK output from MPEG audio decoder
4	R_AOLRCLK	I	I ² S LRCLK input to analog audio DAC
5	RU_AOBCLK	O	I ² S BCLK output from MPEG audio decoder
6	R_AOBCLK	I	I ² S BCLK input to analog audio DAC
7	RU_AODATA	O	I ² S DATA output from MPEG audio decoder
8	R_AODATA	I	I ² S DATA input to analog audio DAC
9	RU_AOCLK	I	I ² S SCLK output from MPEG audio decoder ¹
10	R_AOCLK	O	I ² S SCLK input to analog audio DAC
11	TU_ASCLK	I	I ² S SCLK input to MPEG audio encoder ²
12	T_ASCLK	O	I ² S SCLK output from analog audio ADC
13	TU_ADATA	I	I ² S DATA input to MPEG audio encoder
14	T_ADATA	O	I ² S DATA output from analog audio ADC
15	TU_ALRCK	I	I ² S LRCLK input to MPEG audio encoder
16	T_ALRCK	O	I ² S LRCLK output from analog audio ADC
17	TU_ACLK	I	I ² S BCLK input to MPEG audio encoder
18	T_ACLK	O	I ² S BCLK output from analog audio ADC
19	TU_RESET	I	MPEG encoder Reset. Do not use.

¹ Note that IT IS REQUIRED for the DECODER to work that a correct clock is given to this pin. If an incorrect clock or no clock at all is given, the decoder could stop working during boot or during normal operation. In other words, the decoder WILL NOT WORK if the pins 3 to 10 are left unconnected.

² Note that IT IS REQUIRED for the ENCODER to work that a correct clock is given to this pin. If an incorrect clock or no clock at all is given, the encoder will stop working. In other words, the encoder WILL NOT WORK if the pins 11 to 18 are left unconnected.

CN6 (Digital Audio, FPGA, I/O)			
Pin	Symbol	I/O/P	Description
20	SDA	I/O	I ² C bus data line.
21	TU_PLLTHR	I	MPEG encoder PLL reset. Do not use.
22	SCL	I/O	I ² C bus clock line.
23	FP_DOUT	O	XILINX FPGA Data Out Slave Serial programming line
24	FP_PROG	I	XILINX FPGA Prog Slave Serial programming line
25	FP_DIN	I	XILINX FPGA Data In Slave Serial programming line
26	FP_INIT	I	XILINX FPGA Init Slave Serial programming line
27	FP_CCLK	I	XILINX FPGA Clock Slave Serial programming line
28	FP_DONE	O	XILINX FPGA Done Slave Serial programming line

8. CN7 (ITU656 output)



CN7 connector, viewed from connector solder side.

CN7 (ITU656 output)			
Pin	Symbol	I/O/P	Description
1	ITU_656_O_D0	O	ITU656 output bit 0
2	ITU_656_O_D1	O	ITU656 output bit 1
3	ITU_656_O_D2	O	ITU656 output bit 2
4	ITU_656_O_D3	O	ITU656 output bit 3
5	ITU_656_O_D4	O	ITU656 output bit 4
6	ITU_656_O_D5	O	ITU656 output bit 5
7	ITU_656_O_D6	O	ITU656 output bit 6
8	ITU_656_O_D7	O	ITU656 output bit 7
9	HSync_Out	O	Horizontal Sync Output
10	Field_Out	O	Field Sync Output
11	ITU_656_Clk	O	ITU656 Clock output
12	GNDD	P	Digital Ground

9. Power supplies characteristics

9.1. Boards with the Fujitsu MB86390A MPEG encoder

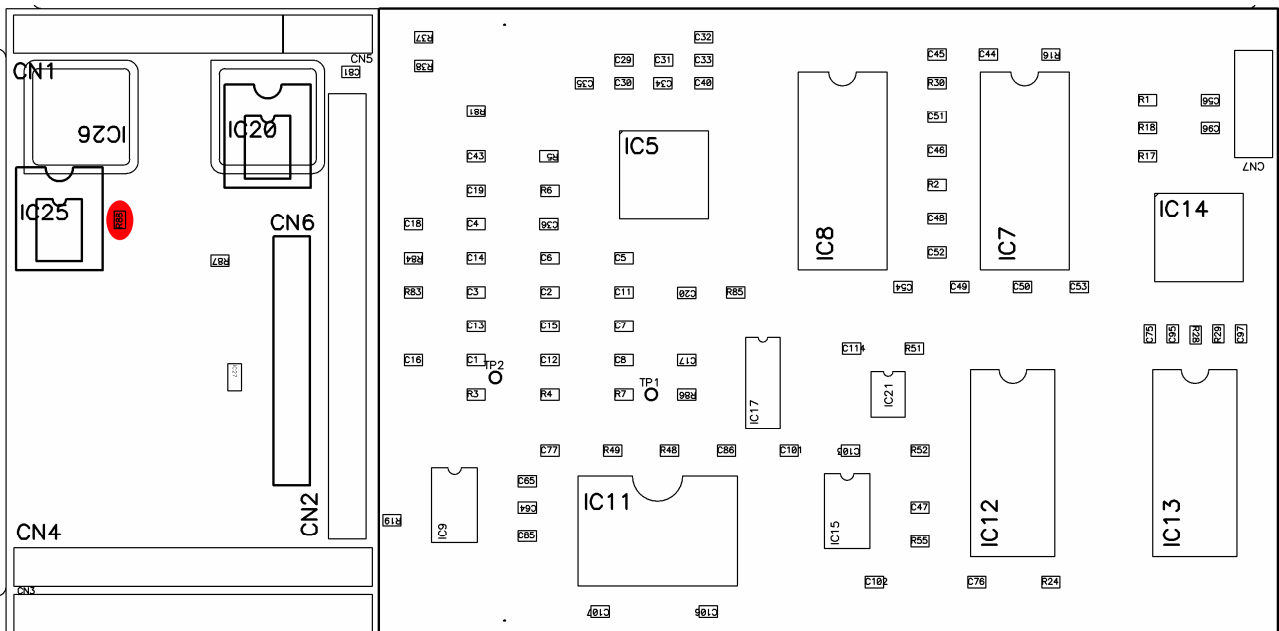
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
2V5	Core voltage			450		mA
3V3	I/O voltage			1		A
5V0	Analog voltage			100		mA

9.2. Boards with the Fujitsu MB86391 MPEG encoder

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
1V8	Core voltage			250		mA
2V5	Core voltage			120		mA
3V3	I/O voltage			1		A
5V0	Analog voltage			100		mA

10. Board layout

10.1. DigiPEG board TOP layout



Highlighted in this figure is resistor R88 to be removed to use the external 27Mhz input for the MPEG encoder.

